What is claimed is:

1. A buffer controller between memories, comprising:

a microprocessor used to process data transmission for the memories;

a first memory connected to the microprocessor; and

a second memory connected to the microprocessor;

wherein the first memory and the second memory transmit data to each other through the microprocessor.

2. The buffer control architecture between memories as in claim 1, further comprising a direct memory access (DMA) connecting among the microprocessor, the first memory and the second memory.

3.The buffer control architecture between memories as in claim 1, further comprising an error correction circuit connecting to the microprocessor, the first memory and the second memory.

4. The buffer control architecture between memories as in claim 1, further comprising a multiplexer connecting to the microprocessor, the first memory and the second memory.

5. The buffer control architecture between memories as in claim 1, wherein the first memory is a flash memory.

6. The buffer control architecture between memories as in claim 1, wherein

the second memory is a static random access memory (SRAM).

7. The buffer control architecture between memories as in claim 1, wherein

the microprocessor is an 8051 chip.

8. The buffer control architecture between memories as in claim 1, wherein the microprocessor further comprises:

a command register used to transmit a write command to the first memory;

an address register used to control a transmission of the address data to the first memory;

a control register used to enable the first memory and control a read/write pulse duration of the first memory;

a data register used to control a data type of the transmission data; and

a data register used to read a state of the first memory.

9. A buffer controlling method between memories comprising steps as follows:

setting a value for a control register to control an enable operation of a memory;

setting a value for a state register to read a data type of the memory; setting a value for a command register to transmit a command data to the memory;

setting a value for an address register to transmit an address signal to the memory;

setting a value for a data register to access the memory; and

setting a value for a state register to read a state of the memory.

10. The buffer control method between memories as in claim 9, further comprising setting the value for the control register to adjust a pulse duration of the read/write signal.

11. The buffer control method between memories as in claim 9, wherein

the address register is an ALEH latch or an ALEL latch.

12. The buffer control method between memories as in claim 9, wherein the value for the data register is selected to determine a transmission data type, and the transmission data type is 8-byte data or 16-byte data.